



# STK820

N-channel 25 V - 0.0058  $\Omega$  - 21 A - PolarPAK<sup>®</sup>  
STripFET<sup>™</sup> Power MOSFET

## Features

Type	V <sub>DSS</sub>	R <sub>DS(on)</sub>	R <sub>DS(on)</sub> *Q <sub>g</sub>	P <sub>TOT</sub>
STK820	25 V	<0.0073 $\Omega$	63 nC*m $\Omega$	5.2 W

- Ultra low top and bottom junction to case thermal resistance
- Very low capacitances
- 100% R<sub>G</sub> tested
- Fully encapsulated die
- 100% matte tin finish (in compliance with the 2002/95/EC european directive)
- PolarPAK<sup>®</sup> is a trademark of VISHAY

## Application

- Switching applications

## Description

This Power MOSFET is the latest development of STMicroelectronics unique “single feature size” strip-based process. The resulting transistor shows extremely high packing density for low on-resistance, moreover the double sides cooling package with ultra low junction to case thermal resistance allows to handle higher levels of current.

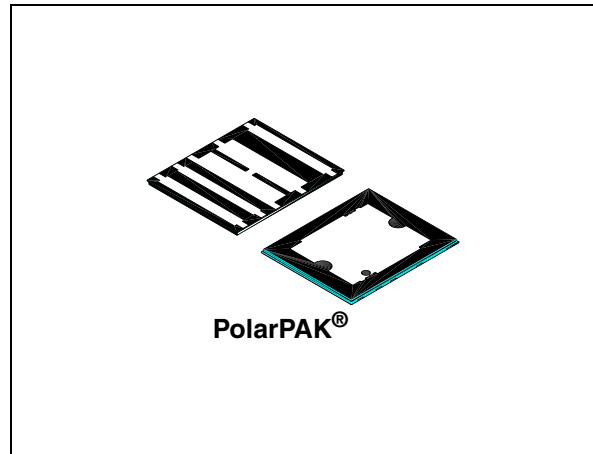


Figure 1. Internal schematic diagram

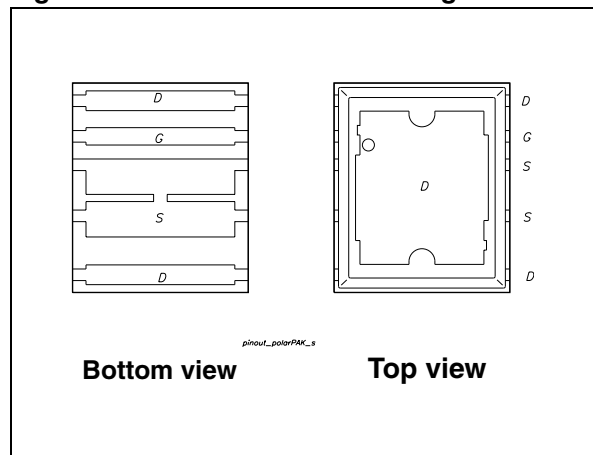


Table 1. Device summary

Order code	Marking	Package	Packaging
STK820	K820	PolarPAK <sup>®</sup>	Tape and reel

# Contents

<b>1</b>	<b>Electrical ratings</b> .....	<b>3</b>
<b>2</b>	<b>Electrical characteristics</b> .....	<b>4</b>
	2.1 Electrical characteristics (curves) .....	6
<b>3</b>	<b>Test circuit</b> .....	<b>8</b>
<b>4</b>	<b>Package mechanical data</b> .....	<b>10</b>
<b>5</b>	<b>Revision history</b> .....	<b>13</b>

# 1 Electrical ratings

**Table 2. Absolute maximum ratings**

Symbol	Parameter	Value	Unit
$V_{DS}$	Drain-source voltage ( $V_{GS} = 0$ )	25	V
$V_{GS}^{(1)}$	Gate-source voltage	$\pm 16$	V
$V_{GS}^{(2)}$	Gate-source voltage	$\pm 18$	V
$I_D^{(4)}$	Drain current (continuous) at $T_A = 25\text{ }^\circ\text{C}$	21	A
$I_D^{(4)}$	Drain current (continuous) at $T_A = 100\text{ }^\circ\text{C}$	13	A
$I_{DM}^{(3)}$	Drain current (pulsed)	84	A
$P_{TOT}^{(4)}$	Total dissipation at $T_A = 25\text{ }^\circ\text{C}$	5.2	W
	Derating factor	0.0416	W/ $^\circ\text{C}$
$E_{AS}^{(5)}$	Single pulse avalanche energy	600	mJ
$T_{stg}$	Storage temperature	-55 to 150	$^\circ\text{C}$
$T_j$	Max. operating junction temperature	150	$^\circ\text{C}$

1. Continuous mode
2. Guaranteed for test time  $\leq 15\text{ ms}$
3. Pulse width limited by package
4. When mounted on FR-4 board of  $1\text{ inch}^2$ , 2 oz Cu and  $\leq 10\text{ sec}$
5. Starting  $T_j = 25\text{ }^\circ\text{C}$ ,  $I_D = 11\text{ A}$ ,  $V_{DD} = 25\text{ V}$

**Table 3. Thermal data**

Symbol	Parameter	Typ.	Max.	Unit
$R_{thj-amb}^{(1)}$	Thermal resistance junction-amb	20	24	$^\circ\text{C/W}$
$R_{thj-c}^{(2)}$	Thermal resistance junction-case (top drain)	1	1.2	$^\circ\text{C/W}$
$R_{thj-c}^{(3)}$	Thermal resistance junction-case (source)	2.8	3.4	$^\circ\text{C/W}$

1. When mounted on FR-4 board of  $1\text{ inch}^2$ , 2 oz Cu and  $\leq 10\text{ sec}$
2. Steady state
3. Measured at source pin when the device is mounted on FR-4 board in steady state

## 2 Electrical characteristics

( $T_{CASE}=25^{\circ}\text{C}$  unless otherwise specified)

**Table 4. On/off states**

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
$V_{(BR)DSS}$	Drain-source breakdown voltage	$I_D = 250 \mu\text{A}$ , $V_{GS} = 0$	25			V
$I_{DSS}$	Zero gate voltage drain current ( $V_{GS} = 0$ )	$V_{DS} = \text{max rating}$ , $V_{DS} = \text{max rating}$ , $T_c = 125^{\circ}\text{C}$			1 10	$\mu\text{A}$ $\mu\text{A}$
$I_{GSS}$	Gate body leakage current ( $V_{DS} = 0$ )	$V_{GS} = \pm 16 \text{ V}$			$\pm 100$	nA
$V_{GS(th)}$	Gate threshold voltage	$V_{DS} = V_{GS}$ , $I_D = 250 \mu\text{A}$	1		2.5	V
$R_{DS(on)}$	Static drain-source on resistance	$V_{GS} = 10 \text{ V}$ , $I_D = 10.5 \text{ A}$ $V_{GS} = 4.5 \text{ V}$ , $I_D = 10.5 \text{ A}$		0.0058 0.0066	0.0073 0.008	$\Omega$ $\Omega$

**Table 5. Dynamic**

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
$C_{iss}$	Input capacitance	$V_{DS} = 25 \text{ V}$ , $f = 1 \text{ MHz}$ , $V_{GS} = 0$		1425		pF
$C_{oss}$	Output capacitance			657		pF
$C_{rss}$	Reverse transfer capacitance			62		pF
$Q_g$	Total gate charge	$V_{DD} = 12.5 \text{ V}$ , $I_D = 21 \text{ A}$		9.5		nC
$Q_{gs}$	Gate-source charge	$V_{GS} = 4.5 \text{ V}$		3.6		nC
$Q_{gd}$	Gate-drain charge	(see Figure 14)		3		nC
$Q_{gs1}$	Pre $V_{th}$ gate-to-source charge	$V_{DD} = 12.5 \text{ V}$ , $I_D = 12 \text{ A}$		2		nC
$Q_{gs2}$	Post $V_{th}$ gate-to-source charge	$V_{GS} = 4.5 \text{ V}$ (see Figure 19)		1.6		nC
$R_G$	Gate input resistance	$f = 1 \text{ MHz}$ Gate DC Bias = 0 Test signal level = 20 mV open drain		0.8		$\Omega$

**Table 6. Switching times**

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
$t_{d(on)}$ $t_r$	Turn-on delay time Rise time	$V_{DD}= 12.5\text{ V}$ , $I_D= 10.5\text{ A}$ , $R_G= 4.7\ \Omega$ , $V_{GS}= 4.5\text{ V}$ (see Figure 16)		15 23		ns ns
$t_{d(off)}$ $t_f$	Turn-off delay time Fall time	$V_{DD}=12.5\text{ V}$ , $I_D= 10.5\text{ A}$ , $R_G= 4.7\ \Omega$ , $V_{GS}= 4.5\text{ V}$ (see Figure 16)		17 4		ns ns

**Table 7. Source drain diode**

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
$I_{SD}$ $I_{SDM}^{(1)}$	Source-drain current Source-drain current (pulsed)				21 84	A A
$V_{SD}^{(2)}$	Forward on voltage	$I_{SD}= 21\text{ A}$ , $V_{GS}= 0$			1.2	V
$t_{rr}$ $Q_{rr}$ $I_{RRM}$	Reverse recovery time Reverse recovery charge Reverse recovery current	$I_{SD}= 21\text{ A}$ , $di/dt = 100\text{ A}/\mu\text{s}$ , $V_{DD}= 20\text{ V}$ , $T_j=150\text{ }^\circ\text{C}$ (see Figure 15)		25 17 1.4		ns nC A

1. Pulse width limited by package
2. Pulsed: pulse duration = 300 $\mu\text{s}$ , duty cycle 1.5%

## 2.1 Electrical characteristics (curves)

Figure 2. Safe operating area

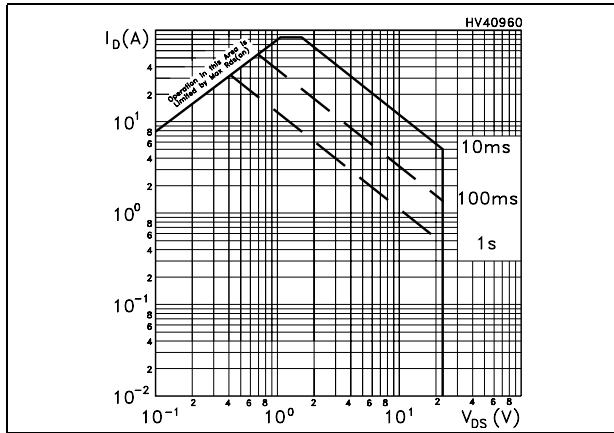


Figure 3. Thermal impedance

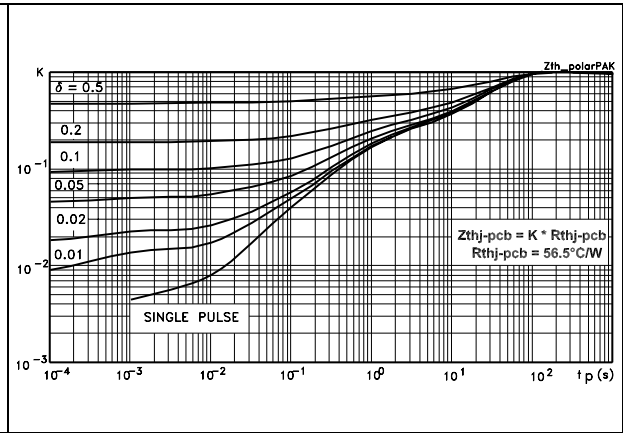


Figure 4. Output characteristics

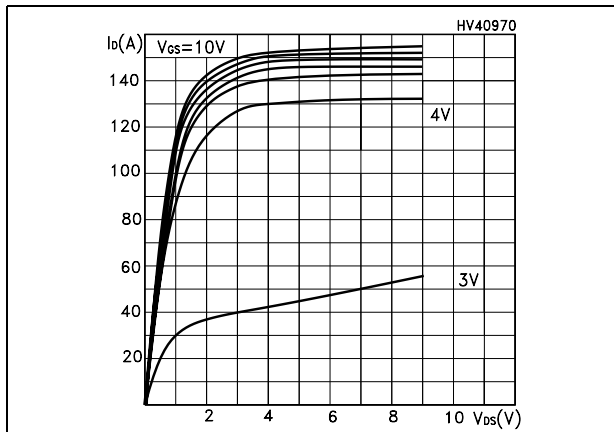


Figure 5. Transfer characteristics

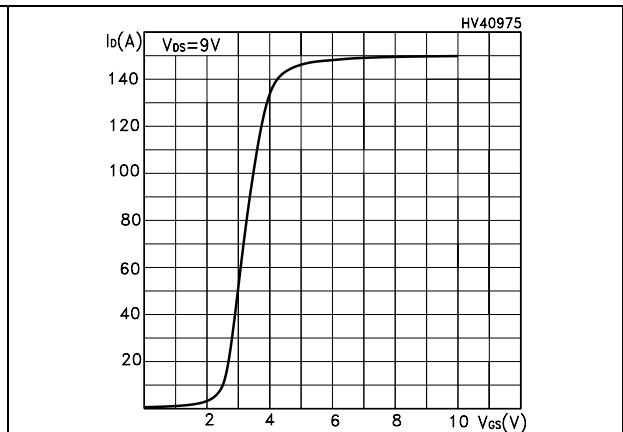


Figure 6. Normalized  $B_{V_{DS}}$  vs. temperature

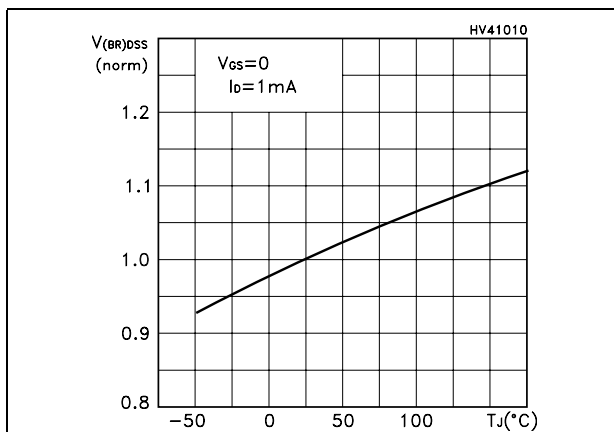


Figure 7. Static drain-source on resistance

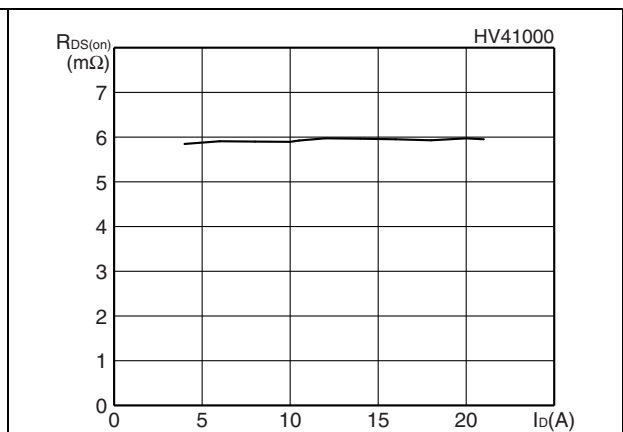


Figure 8. Gate charge vs gate-source voltage Figure 9. Capacitance variations

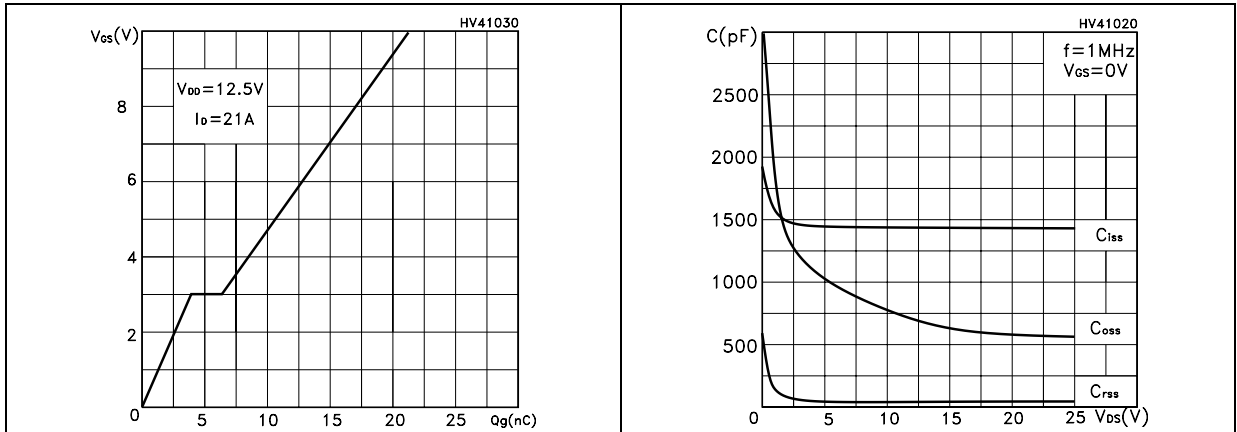


Figure 10. Normalized gate threshold voltage vs temperature Figure 11. Normalized on resistance vs temperature

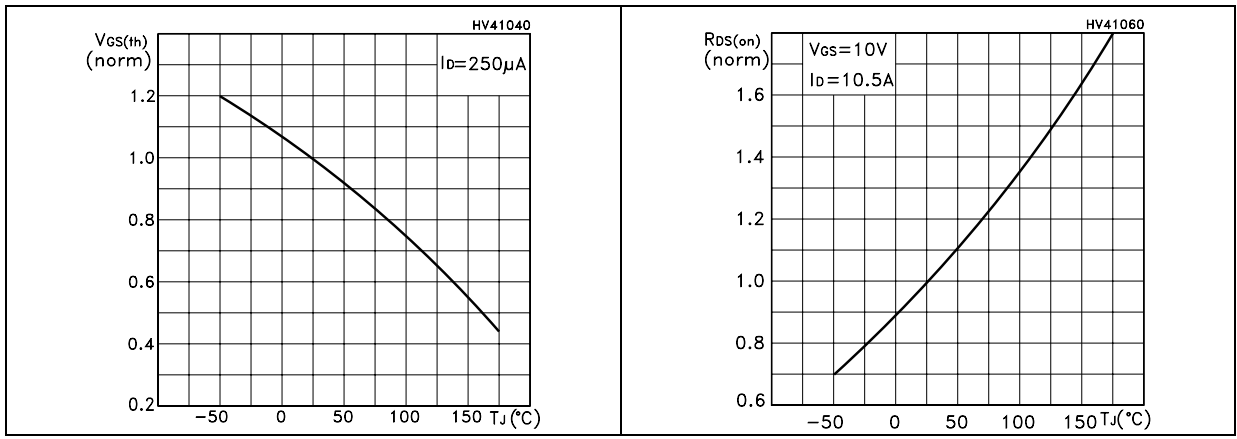
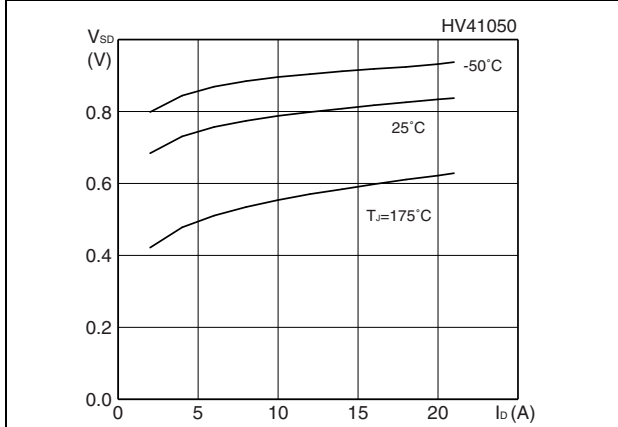


Figure 12. Source-drain diode forward characteristics



### 3 Test circuit

Figure 13. Switching times test circuit for resistive load

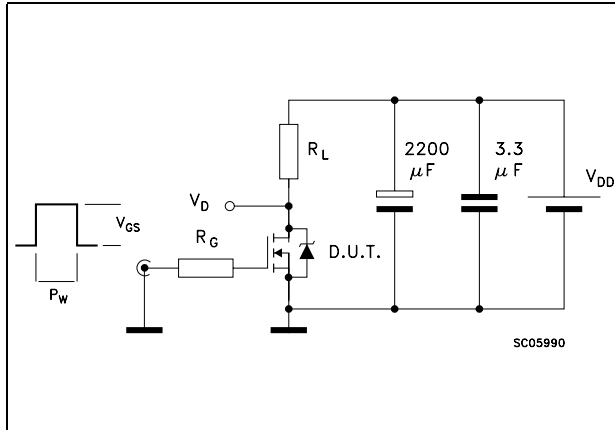


Figure 14. Gate charge test circuit

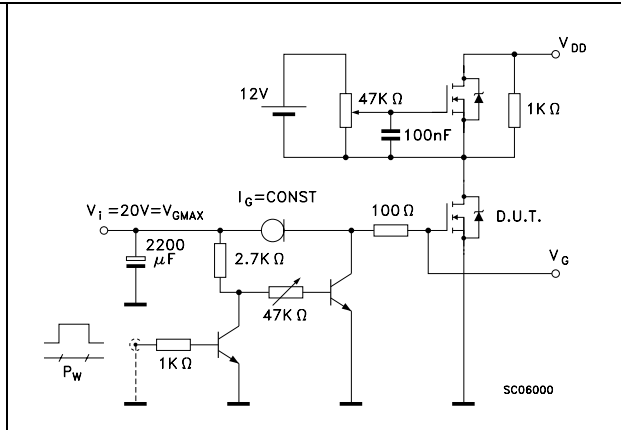


Figure 15. Test circuit for inductive load switching and diode recovery times

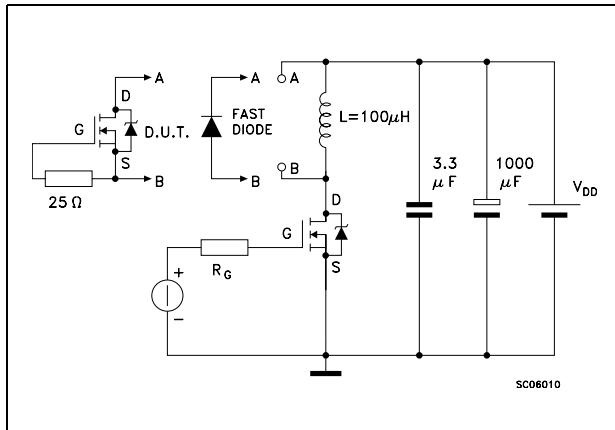


Figure 16. Unclamped inductive load test circuit

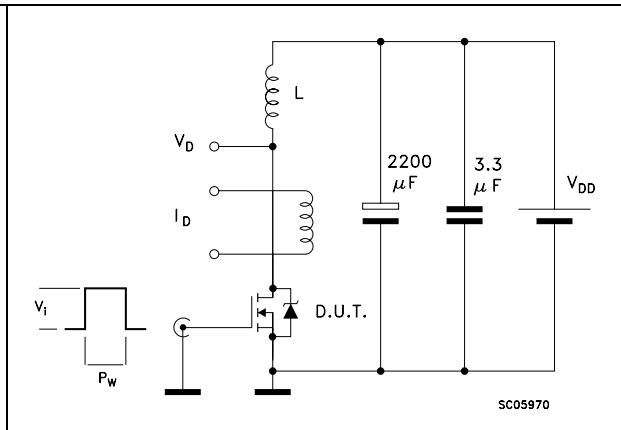


Figure 17. Unclamped inductive waveform

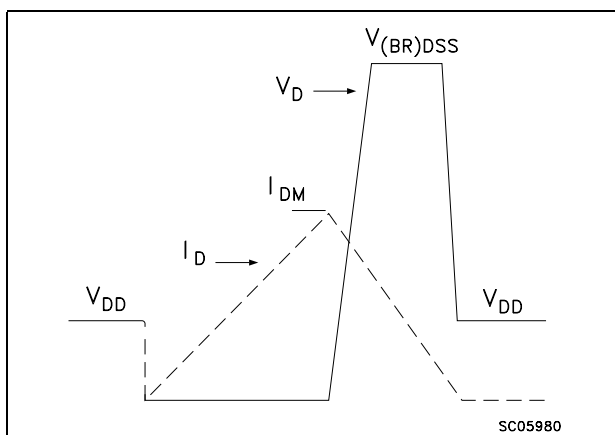


Figure 18. Switching time waveform

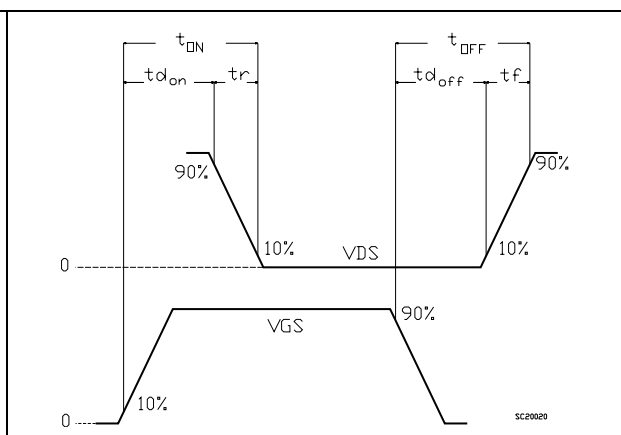
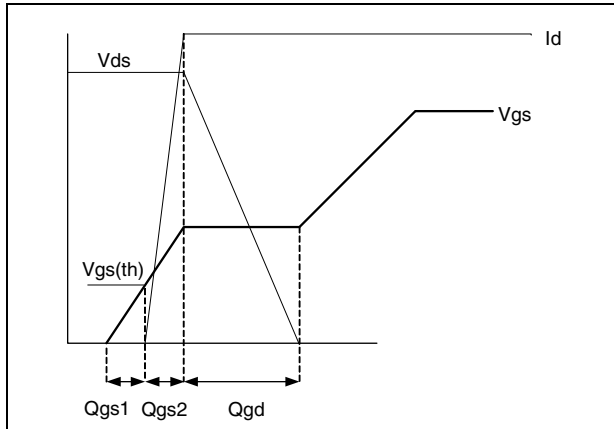




Figure 19. Gate charge waveform



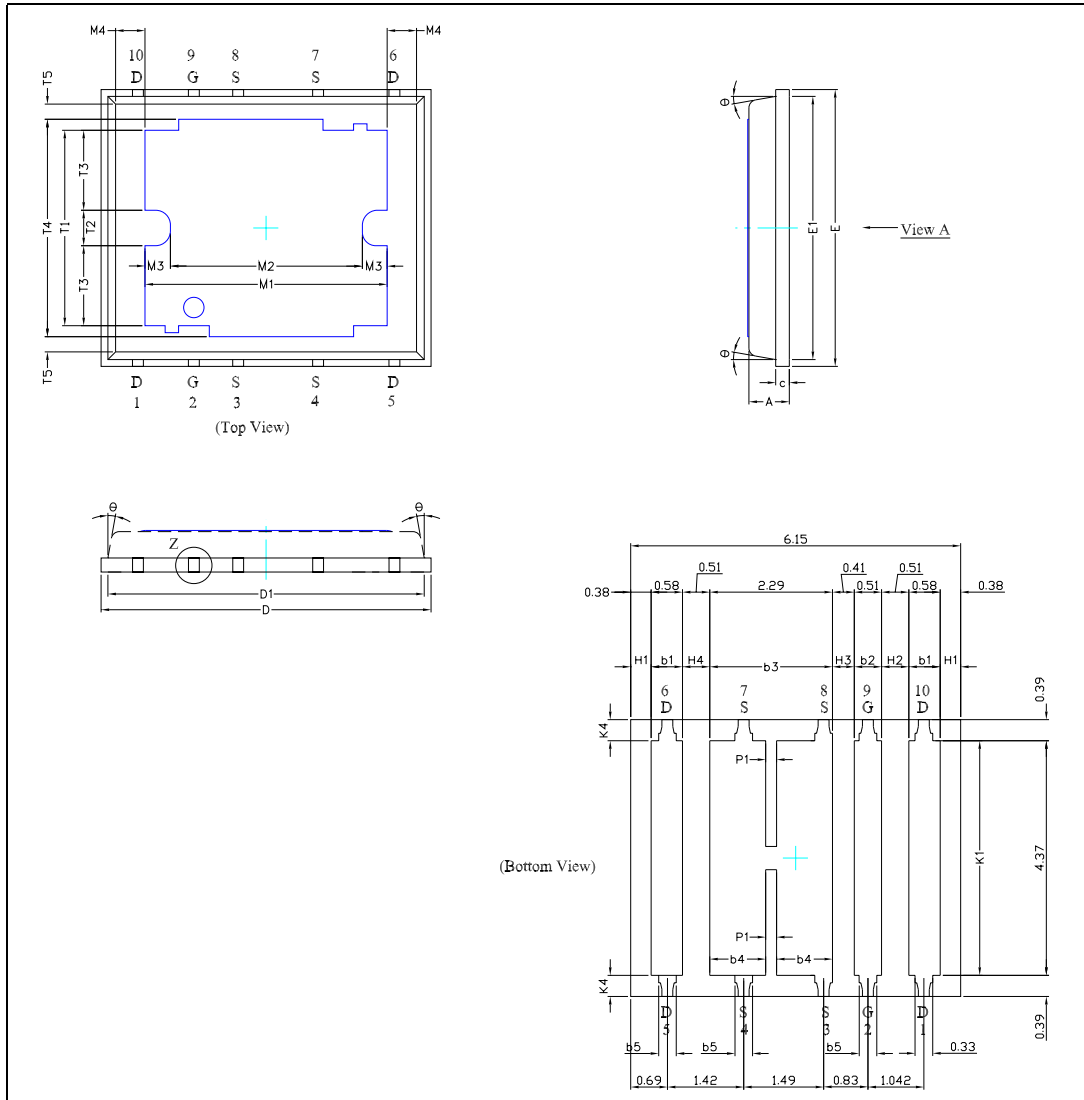
## 4 Package mechanical data

In order to meet environmental requirements, ST offers these devices in ECOPACK® packages. These packages have a Lead-free second level interconnect. The category of second level interconnect is marked on the package and on the inner box label, in compliance with JEDEC Standard JESD97. The maximum ratings related to soldering conditions are also marked on the inner box label. ECOPACK is an ST trademark. ECOPACK specifications are available at: [www.st.com](http://www.st.com)

Table 8. PolarPAK® (option “S”) mechanical data

Ref.	mm			inch		
	Min.	Typ.	Max.	Min.	Typ.	Max.
A	0.75	0.80	0.85	0.030	0.031	0.033
A1			0.05			0.002
b1	0.48	0.58	0.68	0.019	0.023	0.027
b2	0.41	0.51	0.61	0.016	0.020	0.024
b3	2.19	2.29	2.39	0.086	0.090	0.094
b4	0.89	1.04	1.19	0.035	0.041	0.047
b5	0.23	0.33	0.43	0.009	0.013	0.017
c	0.20	0.25	0.30	0.008	0.010	0.012
D	6	6.15	6.30	0.236	0.242	0.248
D1	5.74	5.89	6.04	0.226	0.232	0.238
E	5.01	5.16	5.31	0.197	0.203	0.209
E1	4.75	4.90	5.05	0.187	0.193	0.199
H1	0.23			0.009		
H2	0.45		0.56	0.018		0.022
H3	0.31	0.41	0.51	0.012	0.016	0.020
H4	0.45		0.56	0.018		0.022
I1	1.92	1.97	2.02	0.075	0.077	0.079
J1	0.38	0.43	0.48	0.014	0.016	0.018
K1	4.22	4.37	4.52	0.166	0.172	0.178
K4	0.24			0.009		
M1	4.30	4.50	4.70	0.169	0.177	0.185
M2	3.43	3.58	3.73	0.135	0.141	0.147
M3	0.22			0.009		
M4	0.05			0.002		
P1	0.15	0.20	0.25	0.006	0.008	0.010
T1	3.48	3.64	4.10	0.137	0.143	0.161
T2	0.56	0.76	0.95	0.022	0.030	0.037
T3	1.20			0.047		
T4	3.90			0.154		
T5		0.18	0.36		0.007	0.014
<	0°	10°	12°	0°	10°	12°

Figure 20. PolarPAK® (option “S”) drawings





## 5 Revision history

**Table 9. Document revision history**

Date	Revision	Changes
14-May-2007	1	First version
22-Jun-2007	2	V <sub>DSS</sub> value change in all document
03-Sep-2007	3	Updated mechanical data
19-Dec-2007	4	Document status promoted from preliminary data to datasheet.
14-Feb-2008	5	Updated <a href="#">Table 8</a> , <a href="#">Figure 20</a> and <a href="#">Figure 21</a>

**Please Read Carefully:**

Information in this document is provided solely in connection with ST products. STMicroelectronics NV and its subsidiaries ("ST") reserve the right to make changes, corrections, modifications or improvements, to this document, and the products and services described herein at any time, without notice.

All ST products are sold pursuant to ST's terms and conditions of sale.

Purchasers are solely responsible for the choice, selection and use of the ST products and services described herein, and ST assumes no liability whatsoever relating to the choice, selection or use of the ST products and services described herein.

No license, express or implied, by estoppel or otherwise, to any intellectual property rights is granted under this document. If any part of this document refers to any third party products or services it shall not be deemed a license grant by ST for the use of such third party products or services, or any intellectual property contained therein or considered as a warranty covering the use in any manner whatsoever of such third party products or services or any intellectual property contained therein.

**UNLESS OTHERWISE SET FORTH IN ST'S TERMS AND CONDITIONS OF SALE ST DISCLAIMS ANY EXPRESS OR IMPLIED WARRANTY WITH RESPECT TO THE USE AND/OR SALE OF ST PRODUCTS INCLUDING WITHOUT LIMITATION IMPLIED WARRANTIES OF MERCHANTABILITY, FITNESS FOR A PARTICULAR PURPOSE (AND THEIR EQUIVALENTS UNDER THE LAWS OF ANY JURISDICTION), OR INFRINGEMENT OF ANY PATENT, COPYRIGHT OR OTHER INTELLECTUAL PROPERTY RIGHT.**

**UNLESS EXPRESSLY APPROVED IN WRITING BY AN AUTHORIZED ST REPRESENTATIVE, ST PRODUCTS ARE NOT RECOMMENDED, AUTHORIZED OR WARRANTED FOR USE IN MILITARY, AIR CRAFT, SPACE, LIFE SAVING, OR LIFE SUSTAINING APPLICATIONS, NOR IN PRODUCTS OR SYSTEMS WHERE FAILURE OR MALFUNCTION MAY RESULT IN PERSONAL INJURY, DEATH, OR SEVERE PROPERTY OR ENVIRONMENTAL DAMAGE. ST PRODUCTS WHICH ARE NOT SPECIFIED AS "AUTOMOTIVE GRADE" MAY ONLY BE USED IN AUTOMOTIVE APPLICATIONS AT USER'S OWN RISK.**

Resale of ST products with provisions different from the statements and/or technical features set forth in this document shall immediately void any warranty granted by ST for the ST product or service described herein and shall not create or extend in any manner whatsoever, any liability of ST.

ST and the ST logo are trademarks or registered trademarks of ST in various countries.

Information in this document supersedes and replaces all information previously supplied.

The ST logo is a registered trademark of STMicroelectronics. All other names are the property of their respective owners.

© 2008 STMicroelectronics - All rights reserved

STMicroelectronics group of companies

Australia - Belgium - Brazil - Canada - China - Czech Republic - Finland - France - Germany - Hong Kong - India - Israel - Italy - Japan - Malaysia - Malta - Morocco - Singapore - Spain - Sweden - Switzerland - United Kingdom - United States of America

[www.st.com](http://www.st.com)

